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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,799	HANG, CHIA-LUN	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/30/05* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-58 are presented for examination.

DRAWINGS

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the peripheral devices including controllers must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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SPECIFICATION

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC 112, 1st paragraph

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 43-48 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the processor access the memory arrays, does not reasonably provide enablement for a plurality of peripheral devices writing and reading information out of the memory cells with the peripheral devices including a plurality of controllers connected to the memory banks. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Peripheral devices are not shown or discussed in the present disclosure nor in the drawings.

35 USC § 102

6. The rejection of claims 1-36 as being anticipated by Nakamura is ***maintained*** and repeated below.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

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(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. Claims 1-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura.

9. Nakamura teaches the invention (claim 1) as claimed including a combination comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

a transparent memory array comprising a plurality of memory banks, each of the plurality of memory banks being directly connected to the processor, the memory array operable to function without *at least one of a* precharge signal, a row address latch signal and a column address latch signal during read and write operations. The embedded SDRAM teaches the transparent memory array as a memory array which has a refresh operation for maintaining data in a power down mode without input from a programmer or system designer. The refresh operation is performed using a refresh address counter without supplying the address to the address buffer of the memory array for each cell of the array (e.g., see Figures 6-7 and paragraphs 0069-0077). Specifically, during an internal refresh, addresses and data are not supplied to the arrays, thereby using the refresh counter to supply the addresses needed for refreshing while in the low power mode and not row address signals and column address signals supplied by the address buffer. The direct connection between the processor and the embedded memory arrays is taught as the processor and memory arrays being on the same integrated circuit chip. The element labeled a 'memory controller' shown between the processor and the arrays supplies the same type of circuitry discussed by the Applicant as being necessary for the present invention. Simply labeling this circuitry 'memory controller' does not teach away from the

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direct connectivity. Nakamura does not show it being necessary for multiplexing between the processor and the memory arrays.

As to claim 2, Nakamura teaches the processor simultaneously communicates with at least two of the plurality of memory banks (e.g., see paragraphs 0057-0059). The simultaneous reading and writing of data from/to more than one of the plurality of memory banks is taught as part of a power down mode refresh operation which uses a data input buffer connected to a command latch and controller for each memory bank of the memory array. Figure 2 shows connectivity of element 24 (command latch) from element 13 (command decoder) for each memory bank.

As to claim 3, Nakamura teaches one of the memory banks comprises at least one of a row address decoder, a column address decoder and a controller (e.g., see Figure 2).

As to claim 4, Nakamura teaches the processor provides at least one of a row address signal and a column address signal to the plurality of memory banks, the row address signal having a row address latency period being dependent primarily on a row address decoding pipeline and the column address signal having a column address latency period being dependent primarily on a column address decoding pipeline (e.g., see Figure 2).

As to claim 5, Nakamura teaches on of the plurality of memory banks is a synchronous dynamic random access memory (e.g., see Figure 1 and paragraph 0053).

10. Nakamura teaches the invention (claim 6) as claimed including a combination comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

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a plurality of transparent memory arrays being directly connected to the processor, and each operable to function without *at least one of a* precharge signal, a row address latch signal, and a column address latch signal during read and write operations. The embedded SDRAM teaches the transparent memory array as a memory array which has a refresh operation for maintaining data in a power down mode without input from a programmer or system designer. The refresh operation is performed using a refresh address counter without supplying the address to the address buffer of the memory array for each cell of the array (e.g., see Figures 6-7 and paragraphs 0069-0077). Specifically, during an internal refresh, addresses and data are not supplied to the arrays, thereby using the refresh counter to supply the addresses needed for refreshing while in the low power mode and not row address signals and column address signals supplied by the address buffer. The direct connection between the processor and the embedded memory arrays is taught as the processor and memory arrays being on the same integrated circuit chip. The element labeled a 'memory controller' shown between the processor and the arrays supplies the same type of circuitry discussed by the Applicant as being necessary for the present invention. Simply labeling this circuitry 'memory controller' does not teach away from the direct connectivity. Nakamura does not show it being necessary for multiplexing between the processor and the memory arrays.

As to claim 7, Nakamura teaches the processor simultaneously communicates with at least two of the plurality of transparent memory arrays (e.g., see paragraphs 0057-0059). The simultaneous reading and writing of data from/to more than one of the plurality of memory banks is taught as part of a power down mode refresh operation which uses a data input buffer connected to a command latch and controller for each memory bank of the memory array.

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Figure 2 shows connectivity of element 24 (command latch) from element 13 (command decoder) for each memory bank.

As to claim 8, Nakamura teaches one of the plurality of transparent memory arrays further comprises at least one of a row address decoder, a column address decoder, a controller and a plurality of individual memory cells (e.g., see Figure 2).

As to claim 9, Nakamura teaches the processor provides at least one of a row address signal and a column address signal to the plurality of memory banks, the row address signal having a row address latency period being dependent primarily on a row address decoding pipeline and the column address signal having a column address latency period being dependent primarily on a column address decoding pipeline (e.g., see Figure 2).

As to claim 5, Nakamura teaches on of the plurality of transparent memory arrays is a synchronous dynamic random access memory (e.g., see Figure 1 and paragraph 0053).

11. Nakamura teaches the invention (claim 11) as claimed including a combination comprising:

an integrated circuit having a processor (e.g., see Figure 1, element 2); and,

an embedded memory array, the memory array having a plurality of controllers (e.g., see Figure 2, element 26) and a plurality of memory banks, each of the memory banks being independently connected to one of the plurality of controllers, each of the controllers being independently connected to the processor (e.g., see Figure 2 and paragraphs 0056-0061). Figure 2 shows each memory bank of the memory array has a memory controller, element 26.

As to claim 12, Nakamura teaches the memory array further comprises:

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a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controller (e.g., see Figure 2).

As to claim 13, Nakamura teaches the memory array further comprises a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 14, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see paragraphs 0057-0059).

As to claim 15, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see paragraphs 0057-0059).

As to claim 16, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of row address decoders and the plurality of column address decoders (e.g., see paragraphs 0057-0059).

As to claim 17, Nakamura teaches the embedded memory array is comprised of synchronous dynamic random access memory (e.g., see Figure 1 and paragraph 0053).

12. Nakamura teaches the invention (claim 18) as claimed comprising:

an integrated circuit having a processor (e.g., see Figure 1, element 2); and,

an embedded memory array, the memory array having a plurality of memory banks, each of the memory banks being independently connected to the processor (e.g., see Figure 2 and paragraphs 0056-0061).

As to claim 19, Nakamura teaches the memory array further comprises:

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a plurality of controllers, each of the plurality of controllers being independently connected to the processor (e.g., see Figure 2);

a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2).

As to claim 20, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 21, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see paragraphs 0057-0059).

As to claim 22, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see paragraphs 0057-0059).

As to claim 23, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see paragraphs 0057-0059).

As to claim 24, Nakamura teaches the embedded memory array is comprised of synchronous dynamic random access memory (e.g., see Figure 1 and paragraph 0053).

13. Nakamura teaches the invention (claim 25) as claimed including a combination, comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

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a plurality of transparent SDRAM arrays directly connected to the processor as embedded SDRAM. The embedded SDRAM teaches the transparent memory array as a memory array which has a refresh operation for maintaining data in a power down mode without input from a programmer or system designer. The refresh operation is performed using a refresh address counter without supplying the address to the address buffer of the memory array for each cell of the array (e.g., see Figures 6-7 and paragraphs 0069-0077). Specifically, during an internal refresh, addresses and data are not supplied to the arrays, thereby using the refresh counter to supply the addresses needed for refreshing while in the low power mode and not row address signals and column address signals supplied by the address buffer. The direct connection between the processor and the embedded memory arrays is taught as the processor and memory arrays being on the same integrated circuit chip. The element labeled a 'memory controller' shown between the processor and the arrays supplies the same type of circuitry discussed by the Applicant as being necessary for the present invention. Simply labeling this circuitry 'memory controller' does not teach away from the direct connectivity. Nakamura does not show it being necessary for multiplexing between the processor and the memory arrays.

As to claim 26, Nakamura teaches each of the plurality of transparent SDRAM memory arrays further comprises:

a plurality of memory banks (e.g., see Figure 2);

a plurality of controllers, each of the plurality of controllers being independently connected to the processor and to one of the plurality of memory banks (e.g., see Figure 2);

a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

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a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2).

As to claim 27, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 28, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 29, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 30, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see Figure 1 and paragraph 0053).

14. Nakamura teaches the invention (claim 31) as claimed including a combination comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

a transparent SDRAM having a plurality of memory banks, each of the plurality of memory banks being directly connected to the processor as embedded SDRAM. The embedded SDRAM teaches the transparent memory array as a memory array which has a refresh operation for maintaining data in a power down mode without input from a programmer or system designer. The refresh operation is performed using a refresh address counter without supplying the address to the address buffer of the memory array for each cell of the array (e.g., see Figures 6-7 and paragraphs 0069-0077). Specifically, during an internal refresh, addresses and data are

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not supplied to the arrays, thereby using the refresh counter to supply the addresses needed for refreshing while in the low power mode and not row address signals and column address signals supplied by the address buffer. The direct connection between the processor and the embedded memory arrays is taught as the processor and memory arrays being on the same integrated circuit chip. The element labeled a 'memory controller' shown between the processor and the arrays supplies the same type of circuitry discussed by the Applicant as being necessary for the present invention. Simply labeling this circuitry 'memory controller' does not teach away from the direct connectivity. Nakamura does not show it being necessary for multiplexing between the processor and the memory arrays.

As to claim 32, Nakamura teaches each of the plurality of transparent SRAM memory arrays further comprises:

a plurality of controllers, each of the plurality of controllers being independently connected to the processor and to one of the plurality of memory banks (e.g., see Figure 2);

a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2).

As to claim 33, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 34, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see Figure 1 and paragraph 0053).

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As to claim 35, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 36, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see Figure 1 and paragraph 0053).

35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 37-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura.

17. Nakamura teaches the invention (claim 37) as claimed including a combination comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

Nakamura does not specifically teaches the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

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As to claim 38, Nakamura teaches each of the plurality of transparent SDRAM memory arrays further comprises:

a plurality of controllers, each of the plurality of controllers being independently connected to the processor and to one of the plurality of memory banks (e.g., see Figure 2);

a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2).

As to claim 39, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 40, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 41, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 42, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see Figure 1 and paragraph 0053).

18. Nakamura teaches the invention (claim 43) as claimed including a transparent memory array comprising:

a plurality of memory banks each comprised of a plurality of memory cells (e.g., see Figure 2).

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Nakamura does not specifically teaches a plurality of peripheral devices for writing information into and reading information out of the memory cells, however, this limitation is not supported by the Applicant's disclosure. The specification does reasonably disclose the processor simultaneously accesses more than one memory bank. The reference shows in Figure 2, each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 44, Nakamura teaches the plurality of peripheral devices further comprises:

a plurality of row address decoders, each of the plurality of row address decoders having a row address input bus and a row address output bus, at least one of the plurality of row address decoders having the row address input bus connected to one of the plurality of controllers and having the row address output bus connected to one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060); and,

a plurality of column address decoders, each of the plurality of column address decoders having a column address input bus and a column address output bus at least one of the plurality of column address decoders having the column address input bus connected to at least one of the plurality of controllers and having the column address output bus connected to at least one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

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As to claim 45, Nakamura teaches the plurality of controllers are operable to simultaneously exchange at least one of the address information and data with a processor (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 46, Nakamura teaches the plurality of controllers are operable to simultaneously exchange at least one of the address information and data with the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 47, Nakamura teaches a data bus, the data bus having a plurality of data lines connected with each of the plurality of memory banks, the data bus operable to simultaneously carry data signals from each of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 48, Nakamura teaches at least two of the memory arrays have a different data signal burst mode (e.g., see Figure 2 and paragraphs 0056-0060).

19. Nakamura teaches the invention (claim 49) as claimed including a method for decreasing the access latency of an integrated circuit having a processor and a plurality of embedded memory arrays having a plurality of memory banks, the method comprising:

connecting each of the plurality of memory banks to the processor (e.g., see Figure 2 and paragraphs 0056-0060); and,

Nakamura does not specifically teaches the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous

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access is shown in Figure 2. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 50, Nakamura teaches the connecting step further comprises:

connecting each of the plurality of memory banks to one of a plurality of row address decoders, one of the plurality of row address decoders being connected to the processor(e.g., see Figure 2 and paragraphs 0056-0060); and,

connecting each of the plurality of memory banks to one of a plurality of column address decoders, one of the plurality of column address decoders being connected to the processor (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 51, Nakamura teaches simultaneously accessing step further comprises at least one of:

simultaneously exchanging row address information between the processor and more than one of the plurality of row address decoders (e.g., see Figure 2 and paragraphs 0056-0060);

simultaneously exchanging column address information between the processor and more than one of the plurality of column address decoders (e.g., see Figure 2 and paragraphs 0056-0060); and,

simultaneously exchanging data between the processor and more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

20. Nakamura teaches the invention (claim 52) as claimed including a method for increasing the throughput of an integrated circuit having a processor and a transparent SDRAM array, the transparent SDRAM array having a controller, a data bus and a plurality of memory banks, each

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of the plurality of memory banks being independently connected to the controller, the method comprising at least one of:

Nakamura does not specifically teaches the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 53, Nakamura teaches the simultaneously reading step further comprises:

simultaneously exchanging read address information between the processor and more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060); and,

providing a data signal from the plurality of memory banks to the data bus (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 54, Nakamura teaches the simultaneously writing step further comprises:

simultaneously exchanging write address information between the processor and more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060); and,

providing a data signal from the plurality of memory banks to the data bus (e.g., see Figure 2 and paragraphs 0056-0060).

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As to claim 55, Nakamura teaches each of the memory banks has a row address decoder and a column address decoder associated therewith, the exchanging read address information step further comprises:

transmitting a first row address information from the processor to a first row address decoder (e.g., see Figure 2 and paragraphs 0056-0060);

transmitting a first column address information from the processor to a first column address decoder (e.g., see Figure 2 and paragraphs 0056-0060); and,

simultaneously transmitting at least one of another row address information and column address information from the processor to at least one of another row address decoder and another column address decoder (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 56, Nakamura teaches providing a data signal from the plurality of memory banks to the data bus further comprises:

simultaneously decoding the read address information exchanged between the processor and more than one of the memory banks (e.g., see Figure 2 and paragraphs 0056-0060);

selecting a memory cell within each of the memory banks based on the read address information (e.g., see Figure 2 and paragraphs 0056-0060); and,

simultaneously read the data signal from the selected memory cells within the plurality of memory banks(e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 57, Nakamura teaches each of the memory banks has a row address decoder and a column address decoder associated therewith, the exchanging write address information step further comprises:

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transmitting a first row address information from the processor to a first row address decoder (e.g., see Figure 2 and paragraphs 0056-0060);

transmitting a first column address information from the processor to a first column address decoder (e.g., see Figure 2 and paragraphs 0056-0060); and,

simultaneously transmitting at least one of another row address information and column address information from the processor to at least one of another row address decoder and another column address decoder (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 58, Nakamura teaches providing a data signal from the plurality of memory banks to the data bus further comprises:

simultaneously decoding the write address information exchanged between the processor and more than one of the memory banks (e.g., see Figure 1 and paragraph 0053);

selecting a memory cell within each of the memory banks based on the write address information (e.g., see Figure 1 and paragraph 0053); and,

simultaneously writing the data signal from the selected memory cells within the plurality of memory banks (e.g., see Figure 1 and paragraph 0053).

RESPONSE TO APPLICANT'S REMARKS

21. Applicant's arguments, see the remarks, filed July 27, 2005, with respect to the rejection(s) of claim(s) 37-58 under 35 USC § 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the given interpretation of the claim language.

22. Nakamura teaches embedded technology with the processor, memory controller and SDRAM arrays on the same integrated circuit chip. Having this circuitry on the same

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semiconductor surface or chip provides the direct connectivity required by the claims. The Applicant's specification supplies definitions for direct connectivity in paragraph 0051. The invention as taught by Nakamura teaches this type of connection. Figures 1 and 2 of Nakamura show elements on the same chip. As the memory arrays and the processor are on the same chip the connectivity is direct, only elements also on the semiconductor surface are between the arrays and the processor and although there is circuitry called a memory controller shown in Figure 1 as being between the arrays and the processor, this memory controller has only the same necessary circuitry as that of the Applicant's disclosure. In addition, there is not a multiplexer shown as being needed between the processor and the arrays, the memory controller shown in Figure 1 does not include a multiplexer which meets the Applicant's own requirements for a 'direct connection' for the given elements.

23. As to the reference not teaching the memory array functioning without one of the following:

a precharge signal

a row address latch signal

a column address latch signal during read and write operations.

As the amended language can be interpreted as being a condition of only the column address latch signal and not the precharge signal or the row address latch signal, this language does not read over the Nakamura reference.

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CONCLUSION

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

September 5, 2005

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